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(54) **ORGANIC LIGHT-EMITTING DIODE DISPLAY**

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(71) Applicant: **Samsung Display Co., Ltd.**, Yongin-si (KR)

(72) Inventors: **Juwon Yoon**, Yongin-si (KR); **Sewan Son**, Yongin-si (KR); **Iljeong Lee**, Yongin-si (KR); **Jiseon Lee**, Yongin-si (KR); **Deukmyung Ji**, Yongin-si (KR)

(57) **ABSTRACT**

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An organic light-emitting diode (OLED) display is disclosed. In one aspect, the OLED display includes a substrate, an interlayer insulating layer arranged over the substrate and an OLED arranged over the interlayer insulating layer. The OLED display also includes a source electrode and a drain electrode arranged over the interlayer insulating layer and a via layer arranged over the interlayer insulating layer and having a via hole exposing the source electrode or the drain electrode. The interlayer insulating layer includes a projecting portion which projects toward the OLED in the via hole.

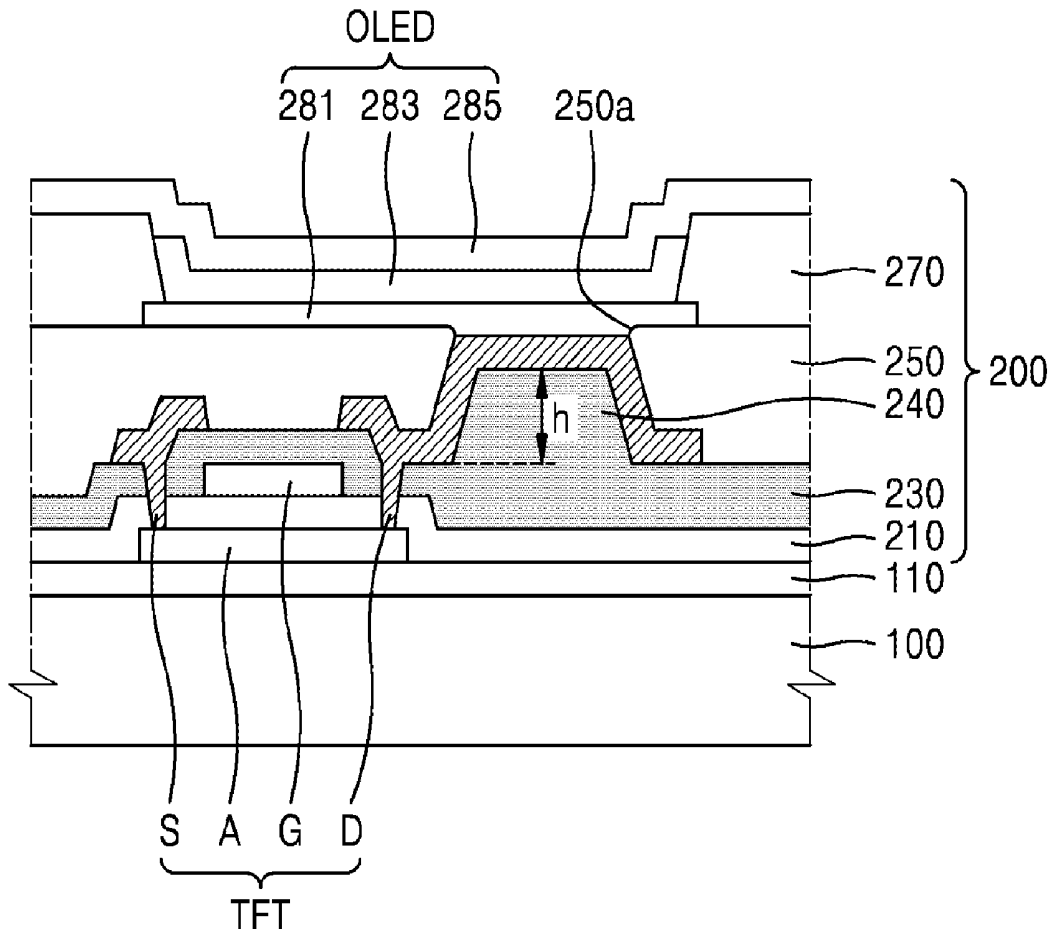


FIG. 1

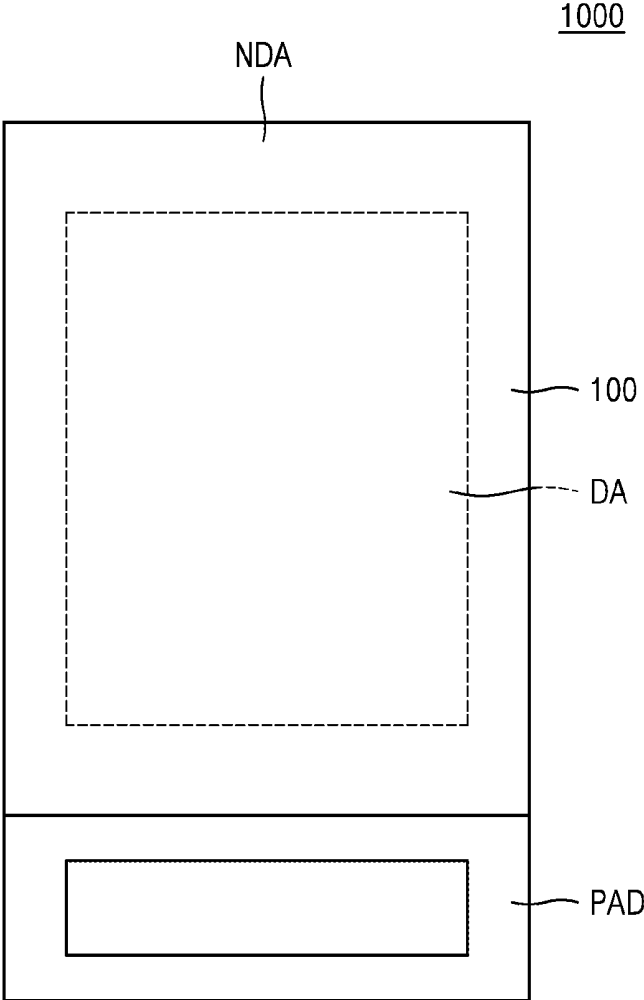


FIG. 2

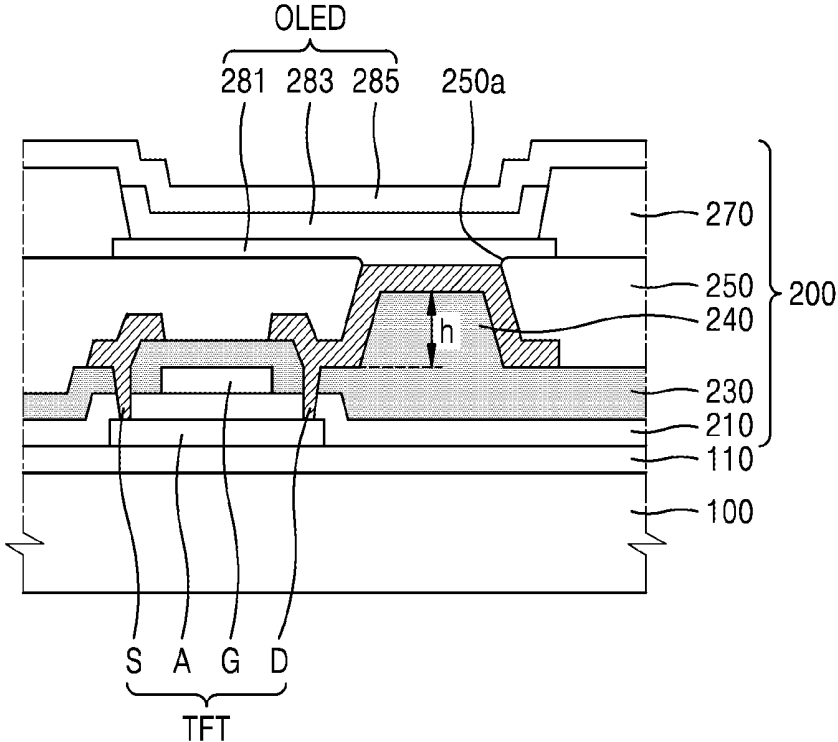
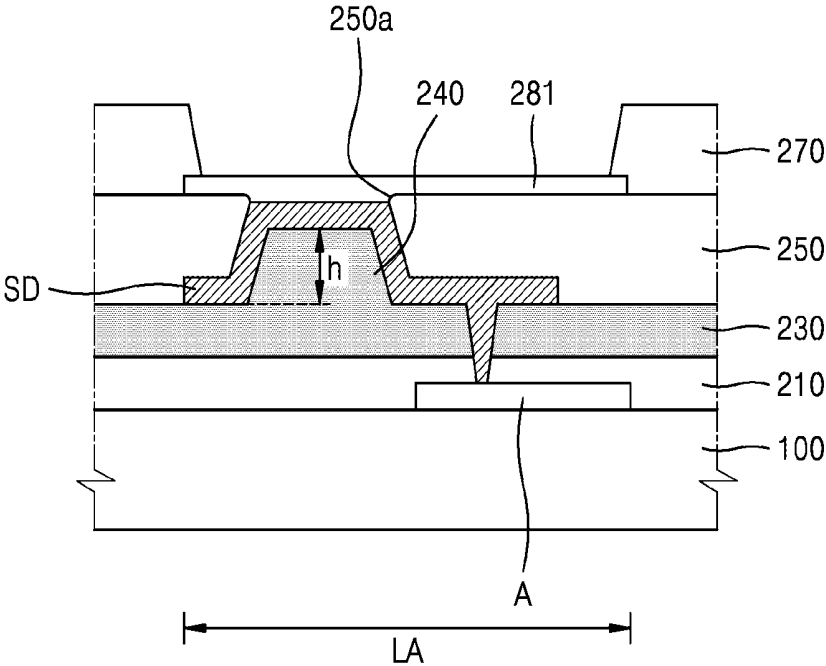


FIG. 3



**ORGANIC LIGHT-EMITTING DIODE
DISPLAY****CROSS-REFERENCE TO RELATED
APPLICATION**

[0001] This application claims the benefit of Korean Patent Application No. 10-2015-0163978, filed on Nov. 23, 2015, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

BACKGROUND

[0002] Field

[0003] The described technology generally relates to an organic light-emitting diode (OLED) display.

[0004] Description of the Related Technology

[0005] An OLED display includes many self-emissive OLEDs each having a hole-injecting electrode, an electron-injecting electrode, and an interposed organic light-emitting layer. The organic light-emitting layer emits light as excitons generated as holes injected by the hole-injecting electrode and electrons injected by the electron-injecting electrode combine with each other in the organic light-emitting layer transit from an excited state to a ground state. Each OLED is driven by a pixel circuit and the combination of OLEDs is used to display images.

[0006] An OLED display has desirable characteristics including a wide viewing angle, high contrast, low power consumption, thin profile, lightweight and fast response speeds. Therefore, OLED technology is being targeted for use in next-generation displays.

**SUMMARY OF CERTAIN INVENTIVE
ASPECTS**

[0007] One inventive aspect relates to an OLED display having an increased aperture ratio.

[0008] Another aspect is an OLED display that includes a substrate, an interlayer insulating layer arranged on the substrate, a source electrode and a drain electrode arranged on the interlayer insulating layer, and a via layer arranged on the interlayer insulating layer and including a via hole exposing the source electrode or the drain electrode, wherein the interlayer insulating layer includes a projecting portion which projects upward in the via hole.

[0009] A part of the source electrode or the drain electrode may be arranged on the projecting portion in the via hole.

[0010] The OLED display may further include a first electrode arranged flat on the via layer without a step.

[0011] A flat lower surface of the first electrode may contact a flat upper surface of the source electrode or the drain electrode in the via hole.

[0012] The source electrode or the drain electrode may include an upper surface which is flush with an upper surface of the via layer in the via hole.

[0013] A height of the projecting portion may be less than that of the via layer.

[0014] A difference between the height of the via layer and that of the projecting portion may be a height of the source electrode or the drain electrode.

[0015] The OLED display may further include a pixel defining layer arranged on the via layer, wherein the pixel defining layer may include an opening exposing a part of the first electrode.

[0016] The projecting portion and one of the source electrode and the drain electrode may be arranged in the via hole.

[0017] Another aspect is an OLED display that includes a substrate, an interlayer insulating layer arranged on the substrate, a source electrode and a drain electrode arranged on the interlayer insulating layer, a via layer arranged on the interlayer insulating layer and including a via hole exposing the source electrode or the drain electrode, and a first electrode arranged flat on the via layer without a step, wherein the interlayer insulating layer may include a projecting portion which projects upward in the via hole.

[0018] Another aspect is an organic light-emitting diode (OLED) display, comprising: a substrate; an interlayer insulating layer arranged over the substrate; an OLED arranged over the interlayer insulating layer; a source electrode and a drain electrode arranged over the interlayer insulating layer; and a via layer arranged over the interlayer insulating layer and having a via hole exposing the source electrode or the drain electrode, wherein the interlayer insulating layer comprises a projecting portion which projects in a direction perpendicular to the substrate in the via hole.

[0019] In the above OLED display, a part of the source electrode or the drain electrode is arranged over the projecting portion in the via hole. The above OLED display further comprises: a first electrode arranged flat on the via layer without a step. In the above OLED display, a flat lower surface of the first electrode contacts a flat upper surface of the source electrode or the drain electrode in the via hole. In the above OLED display, the source electrode or the drain electrode comprises a first upper surface, wherein the distance between the substrate and the first upper surface is the same as the distance between the substrate and an upper surface of the via layer.

[0020] In the above OLED display, the projecting portion has a height less than that of the via layer. In the above OLED display, the interlayer insulating layer includes a body from which the projecting portion projects, and wherein the height of the projecting portion is greater than that of the body. In the above OLED display, the source electrode or the drain electrode has a height which is the same as the difference between the height of the via layer and that of the projecting portion. The above OLED display further comprises: a pixel defining layer arranged over the via layer, wherein the pixel defining layer has an opening exposing a part of the first electrode. In the above OLED display, the projecting portion and one of the source and drain electrodes are arranged in the via hole. In the above OLED display, a top surface of the projecting portion is higher than a top surface of the source or drain electrode.

[0021] In the above OLED display, the source electrode or the drain electrode entirely covers the projecting portion. In the above OLED display, a top surface of the projecting portion is higher than a top surface of the source or drain electrode. The above OLED display further comprises: a thin film transistor (TFT) including the source and drain electrodes and formed over the substrate, wherein the TFT further includes: an active layer formed over the substrate; a gate insulating layer formed on the active layer; and a gate electrode interposed between the gate insulating layer and the interlayer insulating layer, wherein the projecting portion overlaps neither the active layer nor the gate electrode in the depth dimension of the OLED display.

[0022] Another aspect is an organic light-emitting diode (OLED) display, comprising: a substrate; an interlayer insu-

lating layer arranged over the substrate; an OLED arranged over the interlayer insulating layer; a source electrode and a drain electrode arranged over the interlayer insulating layer; a via layer arranged over the interlayer insulating layer and having a via hole exposing the source electrode or the drain electrode; and a first electrode arranged flat over the via layer without a step, wherein the interlayer insulating layer comprises a projecting portion which projects in a direction perpendicular to the substrate in the via hole.

[0023] In the above OLED display, the projecting portion has a height less than that of the via layer. In the above OLED display, the interlayer insulating layer includes a body from which the projecting portion projects, and wherein the height of the projecting portion is greater than that of the body. In the above OLED display, the source electrode or the drain electrode entirely covers the projecting portion.

[0024] Another aspect is an organic light-emitting diode (OLED) display, comprising: a substrate; an interlayer insulating layer arranged over the substrate; an OLED arranged over the interlayer insulating layer; a source electrode and a drain electrode arranged over the interlayer insulating layer; and a via layer arranged over the interlayer insulating layer and having a via hole exposing the source electrode or the drain electrode, wherein the interlayer insulating layer comprises a body and a projection extending from the body in a direction perpendicular to the substrate in the via hole so as to overlap the OLED in the depth dimension of the OLED display.

[0025] In the above OLED display, a top surface of the projection is higher than a top surface of the source or drain electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] These and/or other aspects will become apparent and more readily appreciated from the following description of the embodiments, taken in conjunction with the accompanying drawings.

[0027] FIG. 1 is a plan view of a display device according to one or more embodiments.

[0028] FIG. 2 is a schematic sectional view of the display device illustrated in FIG. 1.

[0029] FIG. 3 is an enlarged sectional view of an interlayer insulating layer and a via layer illustrated in FIG. 2 as a center.

DETAILED DESCRIPTION OF CERTAIN INVENTIVE EMBODIMENTS

[0030] A typical pixel electrode of an OLED display has a step structure that with aging from thermoelectric effects can be degraded. Thus, structural degradation affects the lifetime of the display, and therefore, the light-emitting capability diminishes with time.

[0031] Reference will now be made in detail to embodiments, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to like elements throughout. In this regard, the present embodiments may have different forms and should not be construed as being limited to the descriptions set forth herein. Accordingly, the embodiments are merely described below, by referring to the figures, to explain aspects of the present description. As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed

items. Expressions such as “at least one of” when preceding a list of elements, modify the entire list of elements and do not modify the individual elements of the list.

[0032] Hereinafter, embodiments will be described in detail with reference to the accompanying drawings. The same reference numerals are used to denote the same elements, and repeated descriptions thereof will be omitted.

[0033] It will be understood that although the terms “first”, “second”, etc. may be used herein to describe various components, these components should not be limited by these terms. These components are only used to distinguish one component from another.

[0034] An expression used in the singular encompasses the expression of the plural, unless it has a clearly different meaning in the context.

[0035] Sizes of elements in the drawings may be exaggerated for convenience of explanation. In other words, since sizes and thicknesses of components in the drawings are arbitrarily illustrated for convenience of explanation, the described technology is not limited thereto.

[0036] When a certain embodiment may be implemented differently, a specific process order may be performed differently from the described order. For example, two consecutively described processes may be performed substantially at the same time or performed in an order opposite to the described order.

[0037] In this disclosure, the term “substantially” includes the meanings of completely, almost completely or to any significant degree under some applications and in accordance with those skilled in the art. Moreover, “formed, disposed over positioned over” can also mean “formed, disposed or positioned on.” The term “connected” includes an electrical connection.

[0038] FIG. 1 is a plan view of a display device 1000 according to one or more embodiments.

[0039] The display device includes a substrate 100. The substrate may be formed of various materials with flexibility and may be formed of plastic materials with good heat-resistance and durability.

[0040] The substrate 100 may include a display area DA implementing images that a user may recognize, and a non-display area NDA which is an area outside the display area DA.

[0041] The display area DA may include various elements such as an organic light emitting element and a liquid crystal display element which generating light, and voltage lines supplying electrical power to the display area DA may be arranged in the non-display area NDA.

[0042] In addition, the non-display area NDA may include a pad unit PAD, which may transfer electrical signals from a power supply (not illustrated) or a signal generator (not illustrated) to the display area DA.

[0043] The pad unit PAD may include a driver integrated circuit (IC) (not illustrated), a pad (not illustrated) connecting the driver IC and pixel circuits to each other, and a fan-out wiring (not illustrated).

[0044] FIG. 2 is a schematic sectional view of the display device 1000 illustrated in FIG. 1.

[0045] The display device 1000 includes the substrate 100 and a display unit 200 provided on the substrate 100, according to the present embodiment.

[0046] The substrate 100 may include various materials as described above. In another embodiment, the substrate 100 may include transparent glass materials having SiO₂ as a

main component. However, the described technology is not limited thereto and the substrate **100** may include transparent plastic materials also. The transparent plastic materials may include at least one of insulating organic materials such as polyethersulphone (PES), polyacrylate (PAR), polyetherimide (PEI), polyethylene naphthalate (PEN), polyethylene terephthalate (PET), polyphethylene sulfide (PPS), polyallylate, polyimide, polycarbonate (PC), cellulose triacetate (TAC) and cellulose acetate propionate (CAP).

[0047] The substrate **100** can have a flexible property and thus, may elongate two-dimensionally.

[0048] In another embodiment, the substrate **100** is formed of materials having the Poisson's ratio of about 0.4 or more. The Poisson's ratio denotes the ratio of transverse contraction strain to longitudinal extension strain in the direction of stretching force.

[0049] The flexibility of the substrate **100** may be enhanced and accordingly the display device **1000** may be easily bendable or foldable by ensuring that materials forming the substrate **100** have a Poisson's ratio of about 0.4 or more, that is, the substrate **100** has a good stretching property.

[0050] The display unit **200** may be arranged over the substrate **100**.

[0051] The display unit **200** may emit visible light so that a user may view images thereon. The display unit **200** may include various elements, for example, an organic light-emitting diode OLED or the liquid crystal display element, etc.

[0052] The display unit **200** may include an OLED, and a detailed description thereof will be provided below.

[0053] A buffer layer **110** may be disposed over the substrate **100**. The buffer layer **110** may prevent a dispersion of ions of impurities, prevent an invasion of moisture or outside air, and function as a barrier layer and/or a blocking layer to flatten a surface of the substrate **100**.

[0054] The buffer layer **110** may include an inorganic layer and be arranged over the entire top surface of the substrate **100**.

[0055] A thin film transistor TFT may be arranged over the buffer layer **110**. An active layer A of the thin film transistor TFT may be formed of polysilicon and may include a channel region doped that is not doped with impurities, and a source region and a drain region respectively formed on one side of the channel region and respectively doped with impurities thereon. Impurities may vary depending on a kind of the thin film transistor TFT and may include n-type impurities or p-type impurities.

[0056] A gate insulating layer **210** may be formed on the active layer A after the active layer A has been formed.

[0057] The gate insulating layer **210** may include inorganic materials such as silicon oxides and silicon nitrides, and may include a single layer or layers. The gate insulating layer **210** may play a role of insulating the active layer A and a gate electrode G arranged on the gate insulating layer **210** from each other.

[0058] The gate insulating layer **210** may include an inorganic layer and be arranged on the entire top surface of the substrate **100**.

[0059] A gate electrode G may be formed on the gate insulating layer **210** after the gate insulating layer **210** has been formed. The gate electrode G may be formed via a photolithography process and an etching process.

[0060] Materials for the gate electrode G may include at least one of metals selected from Mo, Al, Pt, Pd, Ag, Mg, Au, Ni, Nd, Ir, Cr, Li, Ca, Ti, W, and Cu.

[0061] An interlayer insulating layer **230** may be formed on the entire surface of the substrate **100** and cover the gate electrode G, after the gate electrode G has been formed.

[0062] The interlayer insulating layer **230** may include inorganic materials. For example, the interlayer insulating layer **230** is metal oxides or metal nitrides. The inorganic materials may include SiO₂, SiN_x, SiON, Al₂O₃, TiO₂, Ta₂O₅, HfO₂ or ZrO₂.

[0063] The interlayer insulating layer **230** may be formed of inorganic materials such as silicon oxides (SiOx) and/or silicon nitrides (SiNx), and may include a single layer or layers. In some embodiments, the interlayer insulating layer **230** may be configured to have a dual structure of SiOx/SiNy or SiNx/SiOy.

[0064] The interlayer insulating layer **230** may include a projecting portion or projection **240**.

[0065] The projecting portion **240** may be a part of the interlayer insulating layer **230** that projects away from the substrate **100**.

[0066] The projecting portion **240** as part of the interlayer insulating layer **230** may have a prescribed height h.

[0067] A detailed description with respect to the projecting portion **240** will be described below.

[0068] A source electrode S and a drain electrode D of the thin film transistor TFT may be arranged on the interlayer insulating layer **230**.

[0069] The source electrode S and the drain electrode D may include at least one of metals selected from Al, Pt, Pd, Ag, Mg, Au, Ni, Nd, Ir, Cr, Li, Ca, Mo, Ti, W and Cu.

[0070] The source electrode S and the drain electrode D may contact the active layer A through contact holes formed in the gate insulating layer **210** and the interlayer insulating layer **230**.

[0071] The source electrode S or the drain electrode D may be formed over the interlayer insulating layer **230** and may cover the projecting portion **240**.

[0072] For example, as a part of the interlayer insulating layer **230** includes the projecting portion **240**, and the source electrode S and the drain electrode D are arranged over the interlayer insulating layer **230**, some parts of the source electrode S or the drain electrode D may be formed over the projecting portion **240**.

[0073] A via layer **250** may be configured to cover the source electrode S and the drain electrode D.

[0074] A first electrode **281** may be formed on the via layer **250**. The first electrode **281** may be connected to the drain electrode D through a via hole **250a** according to an embodiment illustrated in FIG. 2.

[0075] The via layer **250** may be formed of insulating materials. For example, the via layer **250** may include inorganic materials, organic materials or a combination of organic/inorganic materials, have a single or a multilayer structure, and be formed via various deposition methods. In some embodiments, the via layer **250** includes at least one of polyacrylate resin, epoxy resin, phenolic resin, polyamide resin, polyimide resin, unsaturated polyester resin, polyphenylene resin, polyphenylene sulfide resin, and benzocyclobutene (BCB).

[0076] As described above, in the display device 1000, the projecting portion 240 as a part of the interlayer insulating layer 230 may project upward in the via hole 250a according to the present embodiment.

[0077] Furthermore, as the source electrode S or the drain electrode D is arranged over the interlayer insulating layer 230 and covers the projecting portion 240, the projecting portion 240 and the source electrode S or the drain electrode D may completely fill the via hole 250a.

[0078] For example, an upper surface of the via layer 250 is substantially flat.

[0079] According to another embodiment, the projecting portion 240 has a prescribed height h. The height h may be greater than that of a body (non-projecting portion) of the via layer 250 formed below the projecting portion 240.

[0080] According to another embodiment, the height h of the projecting portion 240 is not higher than and is similar to a height of the via layer 250.

[0081] As illustrated in FIG. 2, in the display device 1000, the drain electrode D may be formed on the projecting portion 240 to cover the same, and thus, an upper surface of the drain electrode D covering the projecting portion 240 may be flush with the upper surface of the via layer 250 according to the present embodiment.

[0082] As the upper surface of the drain electrode D covering the projecting portion 240 is flush with the upper surface of the via layer 250, the upper surface of the via layer 250 may be substantially flat in the via hole 250a. For example, as shown in FIG. 2, the distance between the substrate 100 and the upper surface of the drain electrode D covering the projecting portion 240 is substantially the same as the distance between the substrate 100 and the upper surface of the via layer 250.

[0083] The OLED may be arranged over the via layer 250.

[0084] The OLED may include the first electrode 281, an intermediate layer 283 including an organic light emitting layer, and a second electrode 285. In addition, the display device 1000 may further include a pixel defining layer 270.

[0085] Holes and electrons injected from the first and second electrodes 281 and 285 of the OLED may be combined in the organic light emitting layer of the intermediate layer 283 and thus may generate light.

[0086] The first electrode 281 and/or the second electrode 285 may be provided as a transparent electrode or a reflective electrode. When the first and/or second electrode 281 and 285 are provided as a transparent electrode, the transparent electrode may include ITO, IZO, ZnO or In_2O_3 . When the first and/or second electrode 281 and 285 are provided as a reflective electrode, the reflective electrode may include a reflective layer formed of Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir and Cr, or a compound of these metals, and a transparent layer formed of ITO, IZO, ZnO or In_2O_3 . In some embodiment, the first electrode 281 or the second electrode 285 has a structure of ITO/Ag/ITO.

[0087] The intermediate layer 283 may be between the first and second electrodes 281 and 285, and may include the organic light emitting layer.

[0088] The intermediate layer 283 may include the organic light emitting layer and in addition, may further include at least one of a hole injection layer (HIL), a hole transport layer (HTL), an electron transport layer (ETL), and an electron injection layer (EIL). However, the described technology is not limited thereto and the intermediate layer 283

may include the organic light emitting layer and may further include other various functional layers.

[0089] The first electrode 281 may be a pixel electrode.

[0090] According to another embodiment, as illustrated in FIG. 2, a lower surface of the first electrode 281 is substantially flat.

[0091] For example, as the drain electrode D, which is connected to the first electrode 281, is formed on the projecting portion 240 in the via hole 250a, the first electrode 281 may be substantially flat without a step. FIG. 2 illustrates that the drain electrode D is connected to the first electrode 281 according to the present embodiment. However, the described technology is not limited thereto and the source electrode S may be connected to the first electrode 281.

[0092] When the first electrode 281 is formed in the via hole 250a and connected to the source electrode S or the drain electrode D, a step may be formed on the first electrode 281.

[0093] If the first electrode 281 has a step, portion where the step is formed may deteriorate. As a result, the portion where deterioration occurred may not be used as a light-emitting region due to a lifetime of the OLED and reliability of the display device.

[0094] Therefore, the portion where the step is formed in the first electrode 281 may not be used as a light-emitting region, and thus, an aperture ratio may be lowered.

[0095] According to the present embodiment, as the interlayer insulating layer 230 of the display device 1000 has the projecting portion 240 and some parts of the source electrode S or the drain electrode D is formed over the projecting portion 240, a step is not formed on the first electrode 281.

[0096] For example, as not the first electrode 281 but the source electrode S or the drain electrode D is in the via hole 250a and is flush with the upper surface of the via layer 250, the source electrode S or the drain electrode D may be connected to the first electrode 281.

[0097] Therefore, the first electrode 281 may be connected to the source electrode S or the drain electrode D as being formed substantially flat without a step on the via layer 250.

[0098] Deterioration may not occur due to a step of the electrode 281 according to the present embodiment. Therefore, a wider region including the via hole 250a may be used as a light-emitting region.

[0099] The display device may have a wider light-emitting region as the first electrode 281 is formed substantially flat without a step. Therefore, an aperture ratio may increase and a lifetime of the OLED and reliability of the display device may be improved.

[0100] The pixel defining layer 270 may be formed on the via layer 250.

[0101] The pixel defining layer 270 may define a pixel region and a non-pixel region. The pixel defining layer 270 may include an opening exposing a part of the first electrode and may cover the substrate 100. The opening may be a substantial pixel region as an intermediate layer 283 is formed in the opening.

[0102] FIG. 3 is an enlarged sectional view of the interlayer insulating layer 230 and the via layer 250 illustrated in FIG. 2 as a center.

[0103] For convenience of explanation, FIG. 3 illustrates the source electrode S or the drain electrode D of FIG. 2 as a data line SD forming the source electrode S or the drain electrode D.

[0104] As described above, the active layer A and the gate insulating layer 210 may be disposed on the substrate 100, and the interlayer insulating layer 230 may be formed on the gate insulating layer 210.

[0105] The via layer 250 including the data line SD and the via hole 250a may be formed on the interlayer insulating layer 230, and the first electrode 281, which is connected to the data line SD, may be formed on the via layer 250.

[0106] A part of the interlayer insulating layer 230 may include the projecting portion 240 which projects upward.

[0107] According to another embodiment, the projecting portion 240 is formed in the via hole 250a.

[0108] The height h of the projecting portion 240 may be the same as or less than the height of the via layer 250.

[0109] An upper surface of the data line SD on the projecting portion 240 may be flush with the upper surface of the via layer 250.

[0110] As illustrated in FIG. 3, the display device may have the first electrode 281 be formed substantially flat on the via layer 250 without a step according to the present embodiment.

[0111] The upper surface of the via layer 250 and the data line SD may be substantially flat as the projecting portion 240 of the interlayer insulating layer 230 and the data line SD covering the projecting portion 240 are formed in the via hole 250a of the via layer 250. Furthermore, the first electrode 281 formed on the via layer 250 may be connected to the data line SD to be substantially flat without a step.

[0112] Therefore, a wider light-emitting region LA including the via hole 250a may be formed as deterioration due to a step of first electrode 281 does not occur.

[0113] FIG. 3 illustrates that a part of the first electrode 281 on the via layer 250 includes an opening exposing a part of the first electrode 281, wherein the opening corresponds to the light-emitting region LA.

[0114] However, the embodiment of FIG. 3 is only an example and the light-emitting region LA may be further widened.

[0115] The display device may have the first electrode 281 be formed substantially flat on the via layer 250 to be connected to the data line SD without a step according to the present embodiment. Therefore, an aperture ratio may increase and a lifetime of the OLED and reliability of the display device may be improved.

[0116] It should be understood that embodiments described herein should be considered in a descriptive sense only and not for purposes of limitation. Descriptions of features or aspects within each embodiment should typically be considered as available for other similar features or aspects in other embodiments.

[0117] While the inventive technology has been described with reference to the figures, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope as defined by the following claims.

What is claimed is:

1. An organic light-emitting diode (OLED) display, comprising:

a substrate;

an interlayer insulating layer arranged over the substrate;

an OLED arranged over the interlayer insulating layer;

a source electrode and a drain electrode arranged over the interlayer insulating layer; and

a via layer arranged over the interlayer insulating layer and having a via hole exposing the source electrode or the drain electrode,

wherein the interlayer insulating layer comprises a projecting portion which projects in a direction perpendicular to the substrate in the via hole.

2. The OLED display of claim 1, wherein a part of the source electrode or the drain electrode is arranged over the projecting portion in the via hole.

3. The OLED display of claim 1, further comprising:

a first electrode arranged substantially flat on the via layer without a step.

4. The OLED display of claim 3, wherein a flat lower surface of the first electrode contacts a flat upper surface of the source electrode or the drain electrode in the via hole.

5. The OLED display of claim 1, wherein the source electrode or the drain electrode comprises a first upper surface, wherein the distance between the substrate and the first upper surface is the same as the distance between the substrate and an upper surface of the via layer.

6. The OLED display of claim 1, wherein the projecting portion has a height less than that of the via layer.

7. The OLED display of claim 1, wherein the interlayer insulating layer includes a body from which the projecting portion projects, and wherein the height of the projecting portion is greater than that of the body.

8. The OLED display of claim 6, wherein the source electrode or the drain electrode has a height which is the same as the difference between the height of the via layer and that of the projecting portion.

9. The OLED display of claim 1, further comprising:

a pixel defining layer arranged over the via layer,

wherein the pixel defining layer has an opening exposing a part of the first electrode.

10. The OLED display of claim 1, wherein the projecting portion and one of the source and drain electrodes are arranged in the via hole.

11. The OLED display of claim 1, wherein the source electrode or the drain electrode entirely covers the projecting portion.

12. The OLED display of claim 1, further comprising a thin film transistor (TFT) including the source and drain electrodes and formed over the substrate, wherein the TFT further includes:

an active layer formed over the substrate;

a gate insulating layer formed on the active layer; and

a gate electrode interposed between the gate insulating layer and the interlayer insulating layer,

wherein the projecting portion overlaps neither the active layer nor the gate electrode in a direction perpendicular to the substrate.

13. An organic light-emitting diode (OLED) display, comprising:

a substrate;

an interlayer insulating layer arranged over the substrate;

an OLED arranged over the interlayer insulating layer;

a source electrode and a drain electrode arranged over the interlayer insulating layer;

a via layer arranged over the interlayer insulating layer and having a via hole exposing the source electrode or the drain electrode; and

a first electrode arranged flat over the via layer without a step,

wherein the interlayer insulating layer comprises a projecting portion which projects toward the OLED in the via hole.

14. The OLED display of claim **13**, wherein the projecting portion has a height less than that of the via layer.

15. The OLED display of claim **13**, wherein the interlayer insulating layer includes a body from which the projecting portion projects, and wherein the height of the projecting portion is greater than that of the body.

16. The OLED display of claim **13**, wherein the source electrode or the drain electrode entirely covers the projecting portion.

17. An organic light-emitting diode (OLED) display, comprising:

a substrate;

an interlayer insulating layer arranged over the substrate;

an OLED arranged over the interlayer insulating layer;

a source electrode and a drain electrode arranged over the interlayer insulating layer; and

a via layer arranged over the interlayer insulating layer and having a via hole exposing the source electrode or the drain electrode,

wherein the interlayer insulating layer comprises a body and a projection extending from the body in a direction perpendicular to the substrate in the via hole so as to overlap the OLED in the depth dimension of the OLED display.

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专利名称(译)	有机发光二极管显示器		
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[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	YOON JUWON SON SEWAN LEE ILJEONG LEE JISEON JI DEUKMYUNG		
发明人	YOON, JUWON SON, SEWAN LEE, ILJEONG LEE, JISEON JI, DEUKMYUNG		
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摘要(译)

公开了一种有机发光二极管 (OLED) 显示器。在一个方面, OLED显示器包括基板, 布置在基板上方的层间绝缘层和布置在层间绝缘层上方的 OLED。OLED显示器还包括布置在层间绝缘层上方的源电极和漏电极以及布置在层间绝缘层上方并且具有暴露源电极或漏电极的通孔的通孔层。层间绝缘层包括在通孔中朝向OLED突出的突出部分。

